NAGA KUMAR GAJU

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| **Education:** |  |
|  |  |  | January 2017 **–** August2018(Expected) |
| **Texas Tech University, Lubbock, TX** |
| Master of science in Electrical and Computer Engineering | GPA: 3.6 |
| Publication: “*A New Algorithm for Reversible Logic Circuit Synthesis*”, Paper Id: IJERTV7IS020081, Feb 2018, International Journal of Engineering Research & Technology (IJERT), (ISSN: 2278-0181) |
| **Auburn University, Auburn, AL** | August 2016 **–** December 2016 |
| Master of Science in Electrical and Computer Engineering | GPA:3.0 |
| **Sreenidhi Institute of Science and Technology, TG, INDIA** | July 2012 - May 2016 |
| Bachelor of Technology in Electronics and Communication Engineering | GPA: 3.8 |
| **Experience:** |  |
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| **Teaching Assistant** Modern Digital Systems, Texas Tech University March 2017- May 2018* Tutor individual students to complete weekly projects
* Hold discussion groups consisting of a small number of students for the successful completion of course work
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| **Intern Embedded Design,** Electronics Corporation of India Limited-TG, INDIA | June 2015 **–** August 2015 |
| * Worked on Embedded based Security system using RFID to wirelessly identify and grant access for authorized person
* Steered a team of four to successfully complete the project by managing work, organizing meetings and sharinginformation
* Programmed microcontroller AT89C52 using Keil µVision, embedded C and Eagle CAD for PCB design and Fabrication
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| **General Secretary, Bachpan Bachao,** a non-profit organization helping children in need by collecting funds. Feb 2014 – Feb 2016**Certification:**PCB design and fabrication **–** Indo Global Services August 2014**Skills:** |
| **Programming Languages:** C, C++, Python, C#, Data Structures, Java, VHDL, Verilog, System Verilog,Parallel Programming (OpenCL, CUDA), X86 Assembly Language and familiarity with RTL design**Tools and IDEs:** LabVIEW, Xilinx, LT-Spice,Keil µVision, JMP, Silicon Smart, Cadence, NCSim, AWR, MATLAB, VisualStudio, IAR embedded workbench, CodeComposer Studio, QuestaSim, ModelSim**Hardware:** Power Supplies, Oscilloscopes, Multimeter, Signal generator, NI PXIe 1075, NI my-DAQ, Keithley 2400 Series, Keithley 6485, Logic Analyzer, Pico Ammeter, milling machine**Project Experience:****Testing of TL-1963A Low dropout regulator** March 2017-May 2017* Line Regulation, Load Regulation, Dropout voltage, Input reverse leakage and Reverse output current tests are performed on low dropout regulator using Automated Test Equipment (PXI), NI Savage. Code is written in LabVIEW. Cp and Cpk values are obtained from the test measurements using JMP software

**Mixed Signal Characterization and Testing of ADC 7800JU** Jan 2017* Performed various parametric and functional tests on the Mixed Signal IC on PXIe 1075, and bench equipment.
* Developed LabVIEW code and test procedures to test and validate the functionality of DUT with its datasheet. Performed statistical analysis on the data obtained from ATE and bench equipment for its reliability through process capability parameters such as Cp, Cpk and GRR using JMP software

**SVA based Verification of Synchronous FIFO** August 2016-Sept 2016* Developed System Verilog Assertion based verification environment of FIFO buffer operations Push, Pop, Full, Empty, Read and Write. FIFO is synchronous with a single clock governing both read and write operations

**Verification of NAND Flash Controller** Oct 2016-Dec 2016* Designed the verification environment for performance verification of the controller
* Developed a reusable verification environment for performance verification of a NAND Flash Controller Using UVM. The verification environment includes constrained random variable generation, monitors, checkers, assertions and scoreboards to achieve verification goals

**Functional Verification of DDR3 Memory Controller using UVM** July 2017- Oct 2017* Generated Test Cases and Test bench for verifying DDR3 memory controller using CAN controller as master and DDR3 memory controller as a slave
* Developed Cross Domain Clocking block using Asynchronous FIFO. Verified the Read/Write operations of the memory controller

**Design and Implementation of 16-bit RISC ISA processor with pipelining feature**  November 2016* Designed a 16-bit RISC processor using Verilog that can implement a set of instructions and can support pipelining and implementation on FPGA

**Design of an assembler for MSP430G2553 instruction set**  December 2014* Developed code in C++ using Eclipse IDE for a Two pass assembler for MSP430G2553
* Supports a set of 32 instructions of MSP430G2553

**Design of Firmware for TI DSP board** Aug 2017- Dec2017* Developed firmware for TMS320DSK6713 to perform as Equalizer, Filter
* Developed BIOS RTOS for the board

**Image Processing (Noise Reduction, Edge detection and Object identification)** Aug 2016 – Dec 2016* Developed code to read an image using MATLAB and processing it like Noise reduction, Object identification using OpenCL, Message Passing and CUDA scripted in Python

**Implementation of Ensemble meta-algorithm Bagging technique based on Support Vector Machine**  April 2017* Developed code to implement the Bagging technique on a set of data and classify the data using SVM technique
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